



Docket No.: 008089 USA/MTCG/PCTRL

PATENT/OFFICIAL

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Re Application of

Rahul SURANA et al.

Serial No. 10/809,906

Filed: March 26, 2004

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: Group Art Unit:
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: Examiner:

For: A TECHNIQUE FOR PROCESS-QUALIFYING A SEMICONDUCTOR
MANUFACTURING TOOL USING METROLOGY DATA

INFORMATION DISCLOSURE STATEMENT

Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the provisions of 37 C.F.R. 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the documents listed on the attached form PTO-1449. It is respectfully requested that the documents be expressly considered during the prosecution of this application, and that the documents be made of record therein and appear among the "References Cited" on any patent to issue therefrom. Copies of any cited U.S. Patents and U.S. Patent Publications are not being submitted in accordance with 37 CFR 1.98(a)(2)(i).

This Information Disclosure Statement is being filed within three months of the U.S. filing date OR before the mailing date of a first Office Action on the merits. No certification or fee is required.

In accordance with 37 C.F.R. § 1.97(g) and (h), the filing of this IDS should not be construed as a representation that a search had been made or that information cited is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56 (b), or that any cited document listed or attached is (or constitutes) prior art. Unless otherwise indicated, the date of

publication indicated for an item is taken from the face of the item, and Applicant reserves the right to prove that the date of publication is in fact different.

The references listed on Sheet 1 of the attached PTO-1449 Forms were cited in a patentability investigation and/or a corresponding foreign or PCT application relating to the above-referenced application. The remaining references are from potentially related patent applications, and possibly other sources.

No fee is believed to be required; however, the Commissioner is authorized to charge any deficiency in any fees pursuant to 37 CFR § 1.17 associated with this communication and to credit any excess payment to Deposit Account No. 08-0219.

Respectfully submitted,

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INFORMATION DISCLOSURE CITATION IN AN APPLICATION (PTO-1449)				ATTY. DOCKET NO. 008089 USA/MTCG/PCTRL		SERIAL NO. 10/809,906	
				APPLICANT Rahul SURANA et al.			
				FILING DATE March 26, 2004		GROUP	
U.S. PATENT DOCUMENTS							
EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE	
	3,205,485	09/07/65	Noltingk			10/21/60	
	3,229,198	01/11/66	Libby			09/28/62	
	3,767,900	10/23/73	Chao et al.			06/23/71	
	3,920,965	11/18/75	Sohrwardy			03/04/74	
	4,000,458	12/28/76	Miller et al.			08/21/75	
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	5,283,141	02/01/94	Yoon et al.			03/05/92	
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	5,754,297	05/19/98	Nulman			04/14/97	
	5,761,064	06/02/98	La et al.			10/06/95	
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	5,777,901	07/07/98	Berezin et al.			09/29/95	
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	5,808,303	09/15/98	Schlagheck et al.			01/29/97	
	5,812,407	09/22/98	Sato et al.			08/12/97	
	5,823,854	10/20/98	Chen			05/28/96	
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	5,923,553	07/13/99	Yi			10/05/96			
	5,926,690	07/20/99	Toprac et al.			05/28/97			
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	5,943,237	08/24/99	Van Boxem			10/17/97			
	5,960,185	09/28/99	Nguyen			06/24/96			
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	5,961,369	10/05/99	Bartels et al.			06/04/98			
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	6,108,092	08/22/00	Sandhu			06/08/99			
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	6,112,130	08/29/00	Fukuda et al.			10/01/97			
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	09/469,227	12/22/99	Somekh et al.	Multi-Tool Control System, Method and Medium			
	09/619,044	07/19/00	Yuan	System and Method of Exporting or Importing Object Data in a Manufacturing Execution System			
	09/637,620	08/11/00	Chi et al.	Generic Interface Builder			
	09/656,031	09/06/00	Chi et al.	Dispatching Component for Associating Manufacturing Facility Service Requestors with Service Providers			
	09/655,542	09/06/00	Yuan	System, Method and Medium for Defining Palettes to Transform an Application Program Interface for a Service			
	09/725,908	11/30/00	Chi et al.	Dynamic Subject Information Generation in Message Services of Distributed Object Systems			
	09/800,980	03/08/01	Hawkins et al.	Dynamic and Extensible Task Guide			
	09/811,667	03/20/01	Yuan et al.	Fault Tolerant and Automated Computer Software Workflow			
	09/927,444	08/13/01	Ward et al.	Dynamic Control of Wafer Processing Paths in Semiconductor Manufacturing Processes			
	09/928,473	08/14/01	Koh	Tool Services Layer for Providing Tool Service Functions in Conjunction with Tool Functions			
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	10/100,184	03/19/02	Al-Bayati et al.	Method, System and Medium for Controlling Semiconductor Wafer Processes Using Critical Dimension Measurements			
	10/135,405	05/01/02	Reiss et al.	Integration of Fault Detection with Run-to-Run Control			
	10/135,451	05/01/02	Shanmugasundram et al.	Dynamic Metrology Schemes and Sampling Schemes for Advanced Process Control in Semiconductor Processing			
	10/172,977	06/18/02	Shanmugasundram et al.	Method, System and Medium for Process Control for the Matching of Tools, Chambers and/or Other Semiconductor-Related Entities			
	10/173,108	06/18/02	Shanmugasundram et al.	Integrating Tool, Module, and Fab Level Control			
	10/174,370	06/18/02	Shanmugasundram et al.	Feedback Control of Plasma-Enhanced Chemical Vapor Deposition Processes			
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	10/377,654	03/04/03	Kokotov et al.	Method, System and Medium for Controlling Manufacturing Process Using Adaptive Models Based on Empirical Data			
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	10/632,107	08/01/03	Schwarm et al.	Method, System, and Medium for Handling Misrepresentative Metrology Data Within an Advanced Process Control System			
	10/665,165	09/18/03	Paik	Feedback Control of a Chemical Mechanical Polishing Process for Multi-Layered Films			
	10/712,273	11/14/03	Kokotov	Method, System and Medium for Controlling Manufacture Process Having Multivariate Input Parameters			
	10/759,108	01/20/04	Schwarm	Automated Design and Execution of Experiments with Integrated Model Creation for Semiconductor Manufacturing Tools			
	10/765,921	01/29/04	Schwarm	System, Method, and Medium for Monitoring Performance of an Advanced Process Control System			
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	10/809,908	03/26/04	Yang et al.	Improved Control of Metal Resistance in Semiconductor Products via Integrated Metrology			
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						Yes	No
	61-66104	04/04/86	Japan			X	
	61-171147	08/01/86	Japan			X	
	01-283934	11/15/89	Japan			X	
	0 397 924 A1	11/22/90	Europe			X	
	2,050,247	08/29/91	Canada			X	
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	3-202710	09/04/91	Japan			X	
	05-151231	06/18/93	Japan			X	
	05-216896	08/27/93	Japan			X	
	05-266029	10/15/93	Japan			X	
	06-110894	04/22/94	Japan			X	
	06-176994	06/24/94	Japan			X	
	06-184434	07/05/94	Japan			X	
	06-252236	09/09/94	Japan			X	
	06-260380	09/16/94	Japan			X	
	EP 0 621 522 A2	10/26/94	Europe			X	
	WO 95/34866	12/21/95	WO			X	
	8-23166	01/23/96	Japan			X	
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	08-149583	06/07/96	Japan			X	
	08-304023	11/22/96	Japan			X	
	EP 0 747 795 A2	12/11/96	Europe			X	
	09-34535	02/07/97	Japan			X	
	9-246547	09/19/97	Japan			X	
	WO 98/05066	02/05/98	WO			X	
	10-34522	02/10/98	Japan			X	
	10-173029	06/26/98	Japan			X	
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						Yes	No		
	EP 0 869 652 A2	10/07/98	Europe			X			
	WO 98/45090	10/15/98	WO			X			
	EP 0 877 308 A2	11/11/98	Europe			X			
	EP 0 881 040 A2	12/02/98	Europe			X			
	EP 0 895 145 A1	02/03/99	Europe			X			
	WO 99/09371	02/25/99	WO			X			
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	EP 0 910 123 A1	04/21/99	Europe			X			
	11-126816	05/11/99	Japan			X			
	11-135601	05/21/99	Japan			X			
	WO 99/25520	05/27/99	WO			X			
	EP 0 932 194 A1	07/28/99	Europe			X			
	WO 99/59200	11/18/99	WO			X			
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	WO 00/35063	06/15/00	WO			X			
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	EP 1 067 757 A1	01/10/01	Europe			X			
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						Yes	No		
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	WO 01/25865 A1	04/12/01	WO			X			
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		APPLICANT Rahul SURANA et al.	
		FILING DATE March 26, 2004	GROUP
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